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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semi-conductor testing device equipped with the function to detect GURIJJI which appears in more detail in the stimulus impressed to a device, about the semi-conductor testing device for examining the device which is a semiconductor device.
[0002]
[Description of the Prior Art] The configuration of the conventional semi-conductor testing device is shown in drawing 3 . In this drawing, a sign 6 is the device of a test objective. The wave control circuit (format control apparatus) in which the pattern memory by which the generating pattern of a stimulus was programmed, and a sign 4 form the signal wave form of a stimulus based on the generating pattern of a stimulus, and the sign 5 of the timing generator which generates the timing clock of various kinds [sign / 1], the pattern controller by which a sign 2 specifies the generating pattern (pattern-attern) of a stimulus according to the content of a trial, and a sign 3 are input voltage generators which set up the input voltage level (VIH/VIL) of a stimulus.
[0003] Moreover, signs 8 and 9 are relays connected to the input terminal and output terminal of a device 6 of a test objective. The comparison voltage generator and sign 10 which a sign 7 sets up output voltage level (VOH/VOL), and carry out the comparison test of the output signal of a device 6 are a wave control circuit (format control apparatus) which compares an expected-value pattern with the signal wave form from a device 6, and judges the truth of an output signal. In addition, the input voltage level and output voltage level which are set as the input voltage generator 5 and the comparison voltage generator 7, respectively are set up by the test program (with no graphic display) by which the content of a trial was described.
[0004] In this semi-conductor testing device, a timing generator 1 generates the wave formation clock which specifies the timing at the time of the wave control circuit 4 besides a basic clock forming a wave pattern, the strobe which specifies the timing at the time of judging the output signal of a device by the wave formation circuit 10. The pattern controller 2 outputs the address for random pattern generating according to the content of a trial based on the basic clock from a timing generator 1. The pattern memory 3 is outputted to the wave control circuit 4 by using as the impression pattern 13 the random pattern specified in this address. This random pattern is outputted also to the wave control circuit 10 as an expected-value pattern 12.
[0005] The wave control circuit 4 forms the wave pattern which expresses the timing wave of a stimulus based on the impression pattern 13 from the pattern memory 3. The changing point of the logical level of a stimulus, build up time / falling time amount, etc. are reflected in this wave pattern, and the below-mentioned stimulus is specified to it. The input voltage generator 5 makes input voltage level (VIH/VIL) reflect in the wave pattern formed of the wave control circuit 4, and outputs the stimulus (with no sign) which has this input voltage level. This stimulus is given to the input terminal of the device 6 of a test objective through relay 8. A device 6 operates based on this stimulus, and expresses an output signal to that output terminal (with no sign). This output signal is given to the comparison voltage generator 7 through relay 9.
[0006] The comparison voltage generator 7 compares the output signal of a device 6 with the set-up output voltage level (VOH/VOL), judges the logical value of this output signal, and outputs the wave pattern of an output signal. The wave control circuit 10 compares this wave pattern with the expected-value pattern 12, and judges the truth of an output signal. This comparison is performed to the timing specified by the strobe 11 from a timing generator 1. Thus, the stimulus of the programmed pattern is impressed to a device 6 from the input voltage generator 5, and a trial is performed in the output signal of this device 6 as compared with an expected-value pattern.
[0007] Usually, the trial of various items is performed to one device 6, and a test condition is changed during this

trial according to a trial item. In case a test condition is changed, the output of the input voltage generator 5 may become unfixed, the signal which is not meant to a device 6 may be inputted, and a device may be destroyed. Then, in order to avoid such a situation, the relay 8 connected to the output side of the input voltage generator 5 and the relay 9 connected to the input side of the comparison voltage generator 4 are controlled to an OFF state, the terminal of a device 6 is electrically separated from a testing device, and usually changes a test condition.
[0008]
[Problem(s) to be Solved by the Invention] In a place, the following trial item may be performed like [in the case of performing DC trial of the quiescent current etc. after for example AC trial], with the device status held set up by the pattern of a front trial item. Maintaining the relay 8 which gives a stimulus to a device 6 in this case to an ON state, only the on-off condition of the relay 9 of an output side is controlled if needed, and a test condition is changed.
[0009] However, it originates in the relay action performed in case a trial item is changed as mentioned above, and glitzy ****** is carried out and the noise of the shape of a pulse which is not expected to a device 6 may be impressed. When the logical level of the stimulus currently held from the front pattern changes and a device status changes by this glitzy noise, it becomes impossible to examine by the device status to mean. For this reason, starting certain and quick glitzy detection was desired. Although measuring machine machines, such as an oscilloscope, were performing when analyzing such a condition conventionally, the technical problem that much time amount was taken to trace GURIJJI which poses a problem according to this approach occurred.
[0010] This invention solves said technical problem and it aims at obtaining the semi-conductor testing device which can detect certainly and promptly GURIJJI which appears in the stimulus impressed to the device of a test objective.
[0011]
[Means for Solving the Problem] The semi-conductor testing device applied to invention of claim 1 for said object achievement is a semi-conductor testing device which impresses a stimulus to the device of a test objective through a relay, and examines the electrical characteristics of this device, and is characterized by to have a glitzy detection means detect said GURIJJI with reference to the internal signal which specifies said stimulus in the predetermined period set up in order to detect GURIJJI which appears in said stimulus.
[0012] According to this invention, by comparing with the internal signal with which glitzy effect does not reach, the original signal component of a stimulus and the other signal component are distinguished, and signal components other than the signal component of original of a stimulus are detected as a glitzy. As long as it does not specify a stimulus and glitzy effect does not reach, an internal signal may be a wave signal or may be wave information (data). The thing which originated in the internal signal which follows, for example, specifies a stimulus at the relay action and which is not glitzy ******, then GURIJJI which originates in a relay action and appears in a stimulus are detectable.
[0013] A glitzy extract means to extract GURIJJI which the semi-conductor testing device concerning invention of claim 2 compares with said stimulus said 1st reference sign in which said glitzy detection means has a voltage level according to said internal signal, and appears in this stimulus, An inequality detection means to compare said 2nd reference sign which has a logical value according to said internal signal with glitzy ** extracted by said glitzy detection means, and to detect the inequality of these logical values, A detecting-signal output means to output the detecting signal which shows that glitzy ****** of said inequality detection means having detected the inequality was carried out as an opportunity, While generating said 1st and 2nd reference signs, the strobe signal which specifies said predetermined period is generated, and it gives said glitzy extract means and an inequality detection means, and it is characterized by having the control means which controls these glitzy extract means and an inequality detection means.
[0014] According to this invention, a glitzy [a glitzy extract means] when the 1st reference sign which gives the signal level which a stimulus should satisfy is exceeded is considered, and this is extracted. An inequality detection means compares with a glitzy logical value the logical value which a stimulus should satisfy, and detects these inequalities. Here, the logical value of a stimulus does not necessarily change [the glitzy generating direction] with the high-level direction or low-level directions. That is, when regarding that the logical value of a stimulus changes as questionable, it is necessary to not necessarily detect no GURIJJI in the modes. Then, an inequality detection means detects the glitzy existence in the mode to which the logical value of a stimulus is changed by comparing this comparison logic and stimulus with reference to comparison logic. A detecting-signal output means outputs a detecting signal, on condition that this thing [that glitzy ****** was carried out], and glitzy generating hysteresis is made to reflect in a detecting signal, and it leaves it. Therefore, it is supposed that it is possible to detect GURIJJI

with reference to the internal signal which specifies a stimulus, and even after carrying out glitzy ******, glitzy generating can be known ex post.

[0015] The semi-conductor testing device concerning invention of claim 3 is characterized by constituting said control means possible [modification of the time amount location of said strobe signal]. According to this, the time amount location of the predetermined period set up in order to detect glitzy generating can be changed, and glitzy detection can be performed. Therefore, it becomes possible to pinpoint a glitzy time amount location.

[0016]

[Embodiment of the Invention] Hereafter, one gestalt of implementation of this invention is explained to a detail with reference to a drawing. In addition, in each drawing, the same sign is given to the part which is common to the element shown in above-mentioned drawing 3 , and the overlapping explanation is omitted suitably.

[0017] The equipment concerning the gestalt of this operation detects GURIJJI which appears in a stimulus by referring to the internal signal which specifies the stimulus impressed to a device in the predetermined period set up in order to detect GURIJJI resulting from a relay action and to detect this GURIJJI. It explains to a detail below.

[0018] The configuration of the semi-conductor testing device applied to the gestalt of this operation at drawing 1 is shown. In this drawing, a sign 14 is a glitzy detection control circuit as a control means and a detecting-signal output means, and it outputs the detecting signal showing glitzy ****** having been carried out while it controls the comparison voltage generator 15 and comparison circuit 16 which are mentioned later. Moreover, a sign 15 is a comparison voltage generator as a glitzy extract means, and extracts GURIJJI which appears in the stimulus outputted from the input voltage generator 5.

[0019] A sign 16 is a comparison circuit as an inequality detection means, and detects the inequality of a stimulus and the logical value, a glitzy. Moreover, a sign 17 is a processor for control for performing processing about control of a series of glitzy detection actuation. The comparison voltage generator 15 contains the comparator which changes when the output (stimulus) of the input voltage generator 5 is low or high to the below-mentioned comparison electrical potential difference (the 1st reference sign).

[0020] Hereafter, actuation of the semi-conductor testing device concerning the gestalt of this operation is explained, referring to the timing chart shown in drawing 2 . First, in a series of device trials which consist of two or more trial items, after transit of the pattern about a front trial item is completed to the timing shown by drawing 2 (a) and a pre-test is completed, as relay 8 maintains an ON state as it is and shows it in this drawing (b), the stimulus of the trial pattern till then is succeedingly impressed to the input terminal of a device 6.

[0021] At this time, the glitzy detection control circuit 14 incorporates the wave pattern (internal signal) which the wave control circuit 4 outputs, and computes the comparison electrical potential difference (the 1st reference sign) which has a voltage level according to this wave pattern. Moreover, this glitzy detection control circuit 14 generates the comparison logic (the 2nd reference sign) which has the logical level according to this wave pattern, as shown in drawing 2 (d). In addition, as mentioned above, the wave pattern which the wave control circuit 4 outputs specifies a stimulus, and defines the timing and the logical value of a stimulus.

[0022] The comparison electrical potential difference and comparison logic which the glitzy detection control circuit 14 generated are set as the comparison voltage generator 15 and a comparison circuit 16, respectively. After these processings are completed, the glitzy detection control circuit 14 generates the strobe of the window type which specifies a glitzy detection period, as shown in drawing 2 (c). This strobe is generated until the next trial begins.

[0023] The comparison voltage generator 15 compares the comparison electrical potential difference set up by the glitzy detection control circuit 14 with the voltage level of the stimulus outputted from the input voltage generator 5. And as shown in drawing 2 (b), when glitzy G occurs in the output (stimulus) of the input voltage generator 5 and the voltage level exceeds a comparison electrical potential difference, it extracts as a glitzy.

[0024] When the original voltage level of a stimulus is high level (2.4V) for example, in TTL level, specifically, this comparison electrical potential difference is set as 2.0V. In this case, glitzy ****** is carried out when the voltage level of a stimulus becomes less than [2.0V]. Moreover, when the original voltage level of a stimulus is a low level (0.8V) in TTL level, for example, this comparison electrical potential difference is set as 1.0V. In this case, glitzy ****** is carried out when the voltage level of a stimulus becomes more than 1.0V.

[0025] While the glitzy detection control circuit 14 has generated the strobe signal, a comparison circuit 16 supervises the output of the comparison voltage generator 15, and detects glitzy existence. That is, when glitzy G shown in drawing 2 (b) occurs, a comparison circuit 16 compares the comparison logic which was extracted by the comparison voltage generator 15 and which was set up by the glitzy detection control circuit 14 as the glitzy, and when these logical values are inequalities, an inequality signal as shown in drawing 2 (e) is outputted to the glitzy detection control circuit 14.

[0026] If an inequality signal is inputted from a comparison circuit 16, the glitzy detection control circuit 14 will set a detecting signal, as shown in drawing 2 (g). That is, the detecting signal which tells that glitzy G occurred is outputted during the period when the strobe has occurred ignited by the input of an inequality signal. Thereby, even after carrying out glitzy ******, glitzy generating can be known ex post.
[0027] In addition, it is also possible to display that glitzy G occurred on an indicator (with no graphic display) by this detecting signal. Moreover, it can change during the nascent state of the strobe shown in drawing 2 (c) which specifies a glitzy detection period. It enables this to pinpoint the time amount location which glitzy G has generated.
[0028] As mentioned above, although the gestalt of 1 implementation of this invention was explained, this invention is not restricted to this operation gestalt, and even if the design change of the range which does not deviate from the summary of this invention etc. occurs, it is included in this invention. For example, although GURIJJI shall be detected with reference to the wave pattern which the wave control circuit 4 outputs, as long as it is the internal signal with which glitzy effect does not appear and is a signal for specifying a stimulus, without restricting to this, you may be what kind of internal signal. Moreover, although it is a thing resulting from a glitzy ** relay action, without restricting to this, it is based on what kind of cause, and even if a glitzy, it can apply.
[0029]
[Effect of the Invention] As mentioned above, since GURIJJI which appears in this stimulus with reference to the internal signal which specifies said stimulus in the predetermined period set up in order to detect GURIJJI which originates in actuation of a relay and is generated was detected according to this invention, GURIJJI which originates in a relay action etc. by test condition modification, and is generated is promptly [certainly and] detectable.

[Translation done.]